

Module 8

Testing of Embedded System

Version 2 EE-101, Manager 1

Lesson 40

Built-In-Self-Test (BIST) for Embedded Systems

Version 2 EE-101, Manager 2

Instructional Objectives:

After going through this lesson the student would be able to:

- Explain the meaning of the term 'Built-in Self-Test (BIST)'
- Identify the main components of BIST functionality
- Describe the various methods of test pattern generation for designing embedded systems with BIST
- Define what is a Signature Analysis Register and describe some methods to designing such units
- Explain what is a Built-in Logic Block Observer (BLISS) and describe how to use this block for designing BIST

Built-In-Self-Test (BIST) for Embedded Systems

1. Introduction

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT), as illustrated in Figure 40.1 [1]. The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a BIST with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compares and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be exercised through a test controller circuit.

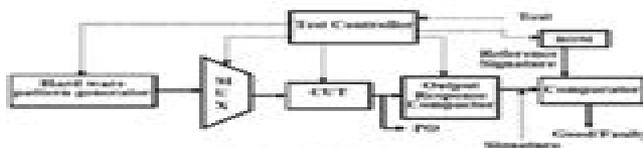


Fig. 40.1 A Typical BIST Architecture

As shown in Figure 40.1, the wires from primary inputs (PIs) to MUX and wires from circuit output to primary outputs (POs) cannot be tested by BIST. In normal operation, the CUT receives its inputs from other modules and performs the functions for which it was designed. During test mode, a test pattern generator circuit applies a sequence of test patterns to the CUT,

and the test responses are evaluated by a output response comparator. In the most common type of BIST, test responses are compared to output response compactors to form faulty signatures. The response signatures are compared with reference golden signatures generated in stored memory, and the correct signal indicates whether chip is good or faulty. First priority parameters must be considered in developing a BIST methodology for embedded systems. These compared with the design parameters for on-line testing techniques discussed in earlier chapter [2].

- **Fault coverage:** This is the fraction of faults of interest that can be exposed by the test patterns produced by pattern generator and detected by output response monitor. In presence of input test patterns errors there is a chance that the compared signatures matches the golden signatures, and the circuit is reported as fault free. This undesirable property is called masking or aliasing.
- **Test set size:** This is the number of test patterns produced by the test generator, and is closely linked to fault coverage; generally, larger test sets imply high fault coverage.
- **Hardware overhead:** The extra hardware required for BIST is considered to be overhead. In most embedded systems, high hardware overhead is not acceptable.
- **Performance overhead:** This refers to the impact of BIST hardware on normal circuit performance such as its worst-case (critical) path delays. Overhead of this type is sometimes more important than hardware overhead.

Issues for BIST

- **Area Overhead:** Additional active area due to test controller, pattern generator, response analyzer and testing of BIST hardware.
- **Pin Overhead:** At least 4 additional pins is needed to activate BIST operation, input MUX, shift write pin, enable.
- **Performance overhead:** Extra path delays are added due to BIST.
- **Yield loss increases:** due to increased chip area.
- **Design effort and time increases:** due to design BIST.
- **The BIST hardware complexity increases:** when the BIST hardware is made variable.

Benefits of BIST

- It reduces testing and maintenance cost, as it requires simpler and less expensive ATE.
- BIST significantly reduces cost of system test pattern generation (LATEP).
- It reduces storage and maintenance of test patterns.
- It can test many units in parallel.
- It makes shorter test application times.
- It can test an functional systems equal.

BIST can be used for non-concurrent, on-line testing of the logic and memory parts of a system [2]. It can readily be configured for event-triggered testing, in which case, the BIST control can be tied to the system reset so that testing occurs during system start-up or shutdown. BIST can also be designed for periodic testing with low fault latency. This requires incorporating a testing process into the CUT that generates the detection of all target faults within a fixed time.

On-line BIST is usually implemented with the main goals of complete fault coverage and low fault latency. Hence, the test generator (TGC) and response monitor (RMC) are generally designed

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Table of Contents Embedded Processorbased Selftest

1. Understanding the eBook Embedded Processorbased Selftest
 - The Rise of Digital Reading Embedded Processorbased Selftest
 - Advantages of eBooks Over Traditional Books
2. Identifying Embedded Processorbased Selftest
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Embedded Processorbased Selftest
 - User-Friendly Interface
4. Exploring eBook Recommendations from Embedded Processorbased Selftest
 - Personalized Recommendations
 - Embedded Processorbased Selftest User Reviews and Ratings
 - Embedded Processorbased Selftest and Bestseller Lists
5. Accessing Embedded Processorbased Selftest Free and Paid eBooks
 - Embedded Processorbased Selftest Public Domain eBooks
 - Embedded Processorbased Selftest eBook Subscription Services
 - Embedded Processorbased Selftest Budget-Friendly Options
6. Navigating Embedded Processorbased Selftest eBook Formats

- ePub, PDF, MOBI, and More
 - Embedded Processorbased Selftest Compatibility with Devices
 - Embedded Processorbased Selftest Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Embedded Processorbased Selftest
 - Highlighting and Note-Taking Embedded Processorbased Selftest
 - Interactive Elements Embedded Processorbased Selftest
 8. Staying Engaged with Embedded Processorbased Selftest
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Embedded Processorbased Selftest
 9. Balancing eBooks and Physical Books Embedded Processorbased Selftest
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Embedded Processorbased Selftest
 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
 11. Cultivating a Reading Routine Embedded Processorbased Selftest
 - Setting Reading Goals Embedded Processorbased Selftest
 - Carving Out Dedicated Reading Time
 12. Sourcing Reliable Information of Embedded Processorbased Selftest
 - Fact-Checking eBook Content of Embedded Processorbased Selftest
 - Distinguishing Credible Sources
 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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